Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A pattern layout method of a semiconductor made in one chip with an anode driver, a cathode driver, and memory portions comprising ~~the steps of~~:

laying out drivers connected to the memory portions equally in the chip, said drivers include a plurality of output regions; and

arranging each memory portion equally in ~~the~~a vicinity of each of the drivers.

2. (Currently Amended) The pattern layout method ~~of a semiconductor device~~ according to claim 1, wherein ~~the~~ desired drivers connected to the memory portions are divided into plural groups and each of the memory portions is ~~arranged~~ provided in every group.

3. (Currently Amended) The pattern layout method ~~of a semiconductor device~~ according to claim 1, wherein the drivers connected to the memory portions are placed face to face at right and left positions or ~~high~~ top and ~~low~~ bottom positions, and each memory portion is arranged at a center portion of the chip.

4. (Currently Amended) The pattern layout method ~~of a semiconductor device~~ according to claim 1, wherein ~~each of the drivers includes a~~ the plurality of output regions constitute an output bit group, each output region ~~corresponding~~corresponds to one bit ~~constituting an output bit group~~, and the method further ~~comprising the step of~~ comprises forming a dummy pattern ~~having the same shape as the output bit to be~~ adjacent to ~~the end portion of~~ the output bit group and having a shape equivalent to the output region.

5. (Currently Amended) The pattern layout method ~~of a semiconductor device~~ according to claim 4, wherein the dummy pattern is formed at an empty space in a region where a plurality of output bits groups are arranged.

6. (Currently Amended) The pattern layout method ~~of a semiconductor device~~ according to claim 4, wherein number of outputs of the dummy pattern formed at a region where output bit groups are adjacent to each other is less than number of outputs of the dummy pattern formed at a region where output bit groups are not adjacent to each other.

7. (Currently Amended) The pattern layout method ~~of a semiconductor device~~ according to claim 4, wherein the dummy pattern has ~~the same~~ a shape equivalent~~as~~to a wiring for gate electrode.

8. (Canceled)

9. (Canceled)

10. (Currently Amended) A pattern layout method of a semiconductor device constituting drivers for driving display where drivers, memory portions are made in one chip, the drivers arranging plural output regions corresponding to one bit to constitute output bit groups, the method comprising ~~the steps of~~:

arranging the drivers at periphery portion in the chip in ~~the~~a state of grouping by every desired output bit group; and

arranging wirings connected to each output bit group of the drivers ~~arranged at the periphery portion~~disposed peripherally to circle ~~fitting shape of~~around within the chip.

11. (Currently Amended) The pattern layout method ~~of a semiconductor device~~ according to claim [10] 19,

wherein the drivers includes an anode driver and a cathode driver, and the drivers are arranged at periphery portions in the chip in a state that one of the anode driver and the cathode driver is grouped by every desired output bit group.

12. (Currently Amended) The pattern layout method ~~of a semiconductor device~~ according to claim [10] 19, wherein the wirings includes a power source line and a signal line.

13. (Currently Amended) The pattern layout method ~~of a semiconductor device~~ according to claim [10] 19 wherein the ~~each of~~ the output bit groups ~~is arranged to~~ surround the memory portions ~~at the periphery portion~~.

14. (Currently Amended) The pattern layout method of a semiconductor device according to claim 10, further comprising ~~the step of~~ forming a dummy pattern ~~having the same shape as the output bit to be~~ adjacent to ~~the end portion of~~ the output bit group and having a shape equivalent to the output region.

15. (Currently Amended) The pattern layout method ~~of a semiconductor device~~ according to claim 14, wherein the dummy pattern is formed at an empty space in a region where a plurality of output bits are ~~arranged~~disposed.

16. (Currently Amended) The pattern layout method ~~of a semiconductor device~~ according to claim 14, wherein number of outputs of the dummy pattern formed at a region where output bit groups are adjacent to each other is less than the number of outputs of the dummy pattern formed at a region where output bit groups are not adjacent to each other.

17. (Currently Amended) The pattern layout method ~~of a semiconductor device~~ according to claim 14, wherein the dummy pattern has ~~the same~~ a shape equivalent ~~as~~to a wiring for gate electrode.

18. (New) A pattern layout method for a semiconductor chip comprising:

laying out an anode driver and a cathode driver equally in the semiconductor chip, each of said drivers containing a plurality of output regions constituting an output bit group, and each output region corresponding to one bit;

providing a memory portion for each of the drivers; and

forming a dummy pattern adjacent to the output bit group, said dummy pattern having a shape equivalent to the output region.

19. (New) A pattern layout method for a semiconductor chip comprising:

disposing drivers at periphery portions of the semiconductor chip, each driver with a plurality of output regions, which constitutes an output bit group, and said output region corresponding to one bit; and

providing wirings for connecting each output bit group of the devices peripherally disposed to circle around within the chip.

20. (New) The pattern layout method according to claim 19, further comprising:

providing memory portions approximately in the center of the semiconductor chip.

Amendments to the Drawings:

The attached replacement sheets of drawings include changes to Figs. 16, 17A, 17B, 17C and 17D and replaces the original sheets including Figs. 16, 17A, 17B, 17C and 17D, respectively.

In Figs. 16, 17A, 17B, 17C and 17D, the legend --Prior Art-- has been added.

Attachments following last page of this Amendment:

Replacement Sheet (2 pages)